be greater than double the doubled clock signal period when the doubled clock signal period is smaller than the delay period.

[0100] It is understood that the specific order or hierarchy of blocks in the processes/flowcharts disclosed is an illustration of exemplary approaches. Based upon design preferences, it is understood that the specific order or hierarchy of blocks in the processes/flowcharts may be rearranged. Further, some blocks may be combined or omitted. The accompanying method claims present elements of the various blocks in a sample order, and are not meant to be limited to the specific order or hierarchy presented.

[0101] The previous description is provided to enable any person skilled in the art to practice the various aspects described herein. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects. Thus, the claims are not intended to be limited to the aspects shown herein, but is to be accorded the full scope consistent with the language claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless specifically so stated, but rather "one or more." The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any aspect described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other aspects. Unless specifically stated otherwise, the term "some" refers to one or more. Combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof" include any combination of A, B, and/or C, and may include multiples of A, multiples of B, or multiples of C. Specifically, combinations such as "at least one of A, B, or C," "at least one of A, B, and C," and "A, B, C, or any combination thereof" may be A only, B only, C only, A and B, A and C, B and C, or A and B and C, where any such combinations may contain one or more member or members of A, B, or C. All structural and functional equivalents to the elements of the various aspects described throughout this disclosure that are known or later come to be known to those of ordinary skill in the art are expressly incorporated herein by reference and are intended to be encompassed by the claims. Moreover, nothing disclosed herein is intended to be dedicated to the public regardless of whether such disclosure is explicitly recited in the claims. No claim element is to be construed as a means plus function unless the element is expressly recited using the phrase "means for."

1. An apparatus for detecting an incorrect clock frequency, the apparatus comprising:

- a first circuit configured to compare a clock signal period to a delay period;
- a second circuit configured to output a first signal, wherein the period of the first signal is double the clock signal period when the clock signal period is greater than the delay period; and
- a third circuit configured to output a second signal, wherein the period of the second signal is greater than double the clock signal period when the clock signal period is less than the delay period.

2. The apparatus of claim **1**, wherein the first circuit, the second circuit, and the third circuit comprise one combined circuit, the combined circuit comprising a frequency sensor circuit including a combination of a delay flip-flop, an inverter, and a delay circuit, an output of the delay flip-flop coupled to an input of the inverter, an output of the inverter coupled to the an input of the delay circuit, and an output of the delay circuit coupled to an input of the delay flip-flop.

3. The apparatus of claim **1**, wherein the first signal and the second signal are both output on the same signal output of a circuit, the first signal output when the clock signal period is greater than the delay period and the second signal output when the clock signal period is less than the delay period.

4. The apparatus of claim **3**, wherein the first signal is output when the clock signal period is equal to the delay period.

5. The apparatus of claim **1**, further comprising a fourth circuit configured to provide a frequency low signal based on the first signal.

6. The apparatus of claim **5**, wherein the fourth circuit comprises a division ratio detection circuit.

7. The apparatus of claim **5**, wherein the frequency low signal is based on a comparison of one or more delayed versions of the first signal, each delayed version of the first signal delayed based on the clock signal.

8. The apparatus of claim **5**, wherein the fourth circuit comprises a division ratio detection circuit.

9. The apparatus of claim **1**, further comprising providing a frequency high signal based on the second signal.

10. The apparatus of claim **9**, wherein the frequency high signal is based on a comparison of one or more delayed versions of the second signal, each delayed version of the second signal delayed based on the clock signal.

11. The apparatus of claim **10**, further comprising a clock doubler configured to double the frequency of the clock signal, wherein:

- the first circuit is further configured to compare the clock signal period of the doubled clock signal to a delay period,
- the second circuit is further configured to output the first signal, wherein the period of the first signal is double the doubled clock signal period when the doubled clock signal period is greater than the delay period; and
- the third circuit is further configured to output the second signal, wherein the period of the second signal is greater than double the doubled clock signal period when the doubled clock signal period is less than the delay period.

12. A method for detecting an incorrect clock frequency, the method comprising:

- comparing a clock signal period to a delay period;
- outputting a first signal, wherein the period of the first signal is double the clock signal period when the clock signal period is greater than the delay period; and
- outputting a second signal, wherein the period of the second signal is greater than double the clock signal period when the clock signal period is less than the delay period.

13. The method of claim **12**, outputting, on a single output, the first signal when the clock signal period is greater than the delay period and outputting, on the single output, the second signal when the clock signal period is less than the delay period.

14. The method of claim **13**, wherein the first signal is output when the clock signal period is equal to the delay period.

15. The method of claim **12**, further comprising outputting a frequency low signal based on the first signal.